2. SGH-E820 Circuit Description

1. SGH-E820 RF Circuit Description

1) RX PART

1. ASM(U100) → Switching Tx, Rx path for GSM900, DCS1800 by logic controlling.

2. ASM Control Logic (Q100, Q102) → Truth Table

	VC1	VC2
GSM Tx Mode	H	L
DCS Tx Mode	L	H
GSM Rx Mode	L	L
DCS Rx Mode	L	L

3. FILTER

Converting electromagnetic field wave to acoustic wave and then pass the specific frequency band.

- GSM FILTER (F101) → For filtering the frequency band between 925 and 960 MHz
- DCS FILTER (F102) → For filtering the frequency band between 1805 and 1880 MHz.

4. VC-TCXO (OSC101)

This module generates the 26MHz reference clock to drive the logic and RF. After additional process, the reference clock applies to the U102 Rx IQ demodulator and Tx IQ modulator. And then, the oscillator is controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. Transceiver (U102)

The receiver front-end which amplifies the GSM, DCS aerial signal, converts the chosen channel down to a low IF signal of 100 kHz. The first stage is composed of symmetrical low noise amplifiers (LNAs). They are matched to 50 ohm. The LNAs are followed by an IQ down mixer. It consists of two mixers in parallel but driven by quadrature out of phase LO signals. The In phase(I) and Quadrature phase(Q) IF signals are low pass filtered to provide protection from high frequency offset interferes. The low IF I and Q signals are then fed into the channel filter. The front-end low IF I and Q outputs enter the integrated bandpass channel filter with provision for five 8 dB gain steps in front of the filter.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U102 chip. OSC100 chip generates modulator signal which power level is about 6.5dBm and fed into Power Amplifier(U101). The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below table.

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-36dBm
		DCS	-36dBm
	400kHz offset 30 kHz bandwidth	GSM	-36dBm
		DCS	-36dBm
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-51dBm
		DCS	-56dBm

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2. Baseband Circuit description of SGH-E820

1. PCF50601 (U400)

1.1. Power Management

Ten low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable boost converter provides support for 1.8V, 3.0V, and 5.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as RTC module and High Voltage Charge pump, Clock generator, aid in reducing both board area and system complexity. I2C BUS serial interface provides access to control and configuration registers. This interface gives a microprocessor full control of the PCF50601 and enables system designers to maximize both standby and talk times.

Supervisory functions. including a reset generator, an input voltage monitor, and a temperature sensor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

1.2. Backlight Brightness Modulator

The Backlight Brightness Modulator (BBM) contains a programmable Pulse-width modulator (PWM) and FET to modulate the intensity of a series of LED's or to control a DC/DC converter that drives LCD backlight.

This phone (SGH-E820) use PWM control to contrast the backlight brigtness.

1.3. Clock Generator

The Clock Generator (CG) generates all clocks for internal and external usage. The 32768 Hz crystal oscillator provides an accurate low clock frequency for the PCF50601 and other circuitry.

2. LCD Connector

LCD is consisted of main LCD(color 65K TFT LCD).

Chip select signals in the U500, LCD_CS, can enable LCD. BACKLIGHT signal enables white LED of main LCD. These signal is from U400.

16-bit data lines(LD(0)~LD(15)) transfers data and commands to LCD. Data and commands use "RS" signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So "L_WR" signal is used to write data or commands to LCD. Power signals for LCD are "LCD_VDD".

3. IRDA

This system uses IRDA module, HSDL_3208, Agilent's. This has signals, "IRDA_DOWN"(enable signal), "RXD0"(input data) and "TXD0"(output data). These signals are connected to OM6359. It uses two power signals. "VDD2" is used for circuit and "VBAT" is used for LED.

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4. Key

This is consisted of key interface pins among OM6359, KBIO(0:7). These signals compose the matrix. Result of matrix informs the key status to key interface in the OM6359. Power on/off key is seperated from the matrix. So power on/off signal is connected with PCF50601 to enable PCF50601. Key LED is consisted of four white LED for sub key and six white LED for main key. Four white LED for sub key use the 3.3V supply voltage. "SUB_BACKLIGHT_KEY_ON" signal enables 3.3V LDO for sub key backlight. Six white LED use the "VDD_KEY" supply voltage.
OM6359 enables six white LED.
"FLIP" informs the status of slide (open or closed) to the OM6359. This uses the hall effect IC, SH248GSP.
A magnet under main LCD enables SH248GSP.

5. EMI ESD Filter

This system uses the EMI ESD filter, EMIF09 to protect noise from IF CONNECTOR part.

6. IF connetor

It is 18-pin connector. They are designed to use VBAT, V_EXT_CHARGE, TXD0, RXD0, RTS0, CTS0, JIG_REC, CHARGER_OK, RXD1, TXD1, AUX_MIC, AUX_SPK and GND. They connected to power supply IC, microprocessor and signal processor IC.

7. Battery Charge Management

A complete constant-current/constant-voltage linear charger for single cell lithium-ion batteries.
If TA connected to phone, "V_EXT_CHARGE" enable charger IC and supply current to battery.
When fault condition caused, "CHG_ON" signal level change low to high and charger IC stop charging process.

8. Audio

EARP_P and EARP_N from OM6359 are connected to the main speaker. AUXSP is connected to the Hands free kit.
MIC_P and MIC_N are connected to the main MIC. And AUX_MIC_P and AUX_MIC_N are connected to earmicrophone.
YMU765_MA5 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.
As a synthesis, YMU765_MA5 is equipped 32 FM voices and 32 Wave Table voices. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects.
Since the play data of YMU765_MA5 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.
YMU765_MA5 includes a speaker amplifier with high ripple removal rate whose maximum output is 580mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor.

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For the purpose of enabling YMU765_MA5 to demonstarte its full capablities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible wiht multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for traning karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU765_MA5 directly interprets and plays blocks relevant to systhesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

9. Memory

Signals in the OM6359 enable two memories. They use only one volt supply voltage, VDD3 in the PCF50601. This system uses Samsung's memory, KBB06B400M-F402. It is consisted of 128M bits flash NOR memory and 256M bits flash NAND memory and 64M bits SCRAM. It has 16 bit data line, HD[0~15] which is connected to OM6359 and MV317SAQ. It has 26 bit address lines, HA[1~26]. CS_NAND and NCSRAM signals is chip select. Writing process, HWR_N is low and it enables writing process to flash memory and SRAM. During reading process, HRD_N is low and it enables reading process to flash memory and SRAM. Each chip select signals in the OM6359 select memory among 2 flash memory and SCRAM. Reading or writing procedure is processed after HWR_N or HRD_N is enabled. Memories use reset, which is VDD3 delay from PCF50601. HA[25] signal enables lower byte of SRAM and HA[26] signal enables higher byte of SRAM.

10. OM6359

OM6359 is consisted of ARM core and DSP core. It has 8x1Kword on-chip program/data RAM, 55 Kwords on-chip program ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of KBS, JTAG, EMI and UART. ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACC(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface.
KBIO(0:7), address lines of DSP core and HD[0~15]. HA[1~26], address lines of ARM core and HD[0~15], data lines of ARM core are connected to memory, YMU765, MV317SAQ(Camera DSP Chip).
CS_NAND, NCSRAM, NCSFLASH in the ARM core are connected to each memory. HWR_N and HRD_N control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as PMU, need the compatible process. KBIO[0~7] receive the status from key and RXD0/TXD0/irDA_DOWN are used for the communications using IRDA and data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).
It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage.

11. VC-TCXO-214C6(26MHz)

This system uses the 26MHz TCXO. AFC control signal forms OM6359 control frequency from 26MHz x-tal. It generates the clock frequency. This clock is connected to UAA3536.

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12. Camera DSP(MV317SAQ)

Tiger is an Integrated circuit for mobile phone camera. This structure will allow effectiveness for large data management and significantly reduces main processor will get burden.

In hence, Tiger will allow the user to be able to display to LCD direct without burdening the main processor. It also allows to have various kinds of display size on the LCD and snapshot for Jpeg. Digital effect will also be executed on real time base resulting Tiger as being a video co-processor in the mobile platform.

Also, an i80 type processor's 16bit parallel interface of Tiger makes it available for the CPU to interchange the data with Tiger. As the additional 8Mbit is usable except 2Mbit buffer embedded in Tiger, the diverse UI data processing which is not a burden to the CPU is available. JPEG encoder and decoder are baseline ISO/IEC 10918-1 JPEG compliance (DCT-based). JPEG decoder supports YUV444, YUV422, YUV420 and YUV411 format standard JPEG image.

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